CLAIMS

1. A voltage level translator for providing an output signal having an external voltage in response to an input signal having an internal voltage, the voltage level translator comprising:

first and second input signal transistors, the gate of the first input signal transistor receiving the input signal, and the gate of the second input signal transistor receiving an input complementary signal;

first and second output signal transistors,

the drain of the first output signal transistor connected to the gate of the second output signal transistor, the drain of the first input signal transistor, and to an output complementary signal node,

the drain of the second output signal transistor connected to the gate of the first output signal transistor, the drain of the second input signal transistor, and to an output signal node; and

a signal stabilization circuit connected to the drains of the first and second input signal transistors to modify a pulse parameter of the output signal at the output signal node.

2. The voltage level translator of claim 1, wherein the signal stabilization circuit comprises first and second signal stabilization transistors, the drain of the first signal stabilization transistor connected to the drain of the first input signal transistor, and the drain of the second signal stabilization transistor connected to the drain of the second input signal transistor.

3. The voltage level translator of claim 2, wherein the sources of the first and second signal stabilization transistors are connected to an internal voltage supply.

4. The voltage level translator of claim 3, wherein the gate of the first signal stabilization transistor receives the input signal, and the gate of the second signal stabilization transistor receives the input complementary signal.

5. The voltage level translator of claim 3, wherein the first and second signal stabilization transistors are low voltage PMOS transistors.

6. The voltage level translator of claim 1, wherein the first and second output signal transistors are PMOS transistors.

7. The voltage level translator of claim 6, wherein the first and second output signal transistors are high voltage transistors.

8. The voltage level translator of claim 1, wherein the first and second input signal transistors are NMOS transistors.

9. The voltage level translator of claim 8, wherein the first and second input signal transistors are low voltage transistors.

10. The voltage level translator of claim 9, further comprising first and second high voltage transistors that each have essentially zero threshold voltage and mediate the connections between the first and second input signal transistors and the first and second output signal transistors.

11. The voltage level translator of claim 9, further comprising a cascode circuit that protects the drains of the first and second input signal transistors from the external voltage.

12. A voltage level translator for providing an output signal having an external voltage in response to an input signal having an internal voltage, the voltage level translator comprising:

first and second input signal transistors, the gate of the first input signal transistor receiving the input signal, and the gate of the second input signal transistor receiving an input complementary signal;

first and second output signal transistors,

the drain of the first output signal transistor connected to the gate of the second output signal transistor, to the drain of the first input signal transistor, and to an output complementary signal node,

the drain of the second output signal transistor connected to the gate of the first output signal transistor, to the drain of the second input signal transistor, and to an output signal node; and

an enable circuit having a first state that connects an external voltage supply to the sources of the first and second output signal transistors, and a second state that isolates the external voltage supply from the sources of the first and second output signal transistors in response to a signal that indicates the readiness of an internal voltage supply.

13. The voltage level translator of claim 12, wherein the enable circuit comprises first and second high voltage PMOS transistors having gates that receive the signal indicating that the internal voltage supply is ready.

14. The voltage level translator of claim 12, further comprising a ready-signal generation circuit that delivers an external high voltage signal to the enable circuit to indicate that the internal voltage supply is ready.

15. The voltage level translator of claim 12, further comprising first and second high voltage transistors that each have essentially zero threshold voltage, and that mediate the connection between the first and second input signal transistors and the first and second output signal transistors.

16. The voltage level translator of claim 12, further comprising a signal stabilization circuit connected to the drains of the first and second input signal transistors to modify a pulse parameter of the output signal at the output signal node.

17. A ready-signal generation circuit for providing a ready-signal indicating that a voltage supply is at an operating voltage, the circuit comprising:

a pair of input transistors, the gate of a first input transistor of the pair of input transistors receiving the input signal, and the gate of a second input transistor of the pair of input transistors receiving an input complementary signal; and

a pair of output transistors,

the drain of a first output transistor of the pair of output transistors connected to the gate of a second output transistor of the pair of output transistors, to the drain of the first input transistor, and to an output complementary signal node,

the drain of the second output transistor connected to the gate of the first output transistor, to the drain of the second input transistor, and to an output signal node,

wherein at least one of the pairs of input transistors and output transistors are unbalanced.

18. The ready-signal generation circuit of claim 17, wherein a resistive element connected in parallel with one transistor of the input and output transistors at least in part causes the at least one unbalanced pair to be unbalanced.

19. The ready-signal generation circuit of claim 17, wherein the at least one unbalanced pair has a parameter selected to at least in part cause the at least one unbalanced pair to be unbalanced.

20. The ready-signal generation circuit of claim 17, further comprising first and second high voltage transistors that each have essentially zero threshold voltage, and that mediate the connections between the pair of input signal transistors and the pair of output signal transistors.